

Amendments to the Claims

The following listing of the claims will replace all prior versions, and listings of the claims in the application:

Listing of Claims

1-8 Canceled

9. (Currently amended) A switch based upon a plurality of opto-electrical-physical implementation levels comprising:

a first switching fabric having a configuration based on a first one of the implementation levels, and

a second switching fabric, coupled to the first switching fabric, having a configuration based on a second one of the implementation levels different from the first one of the implementation levels and compatible with the first switching fabric.

10. (Previously presented) The switch as recited in claim 9 wherein the implementation levels include:

inside-chip implementation, printed circuit board implementation, orthogonal packaging, interface-board packaging, and fiber-array packaging.

11. (Currently amended) A switch based upon a plurality of opto-electrical-physical implementation levels, said switch being constructed from other than a Banyan type of network, said switch comprising:

a first switching element being a primitive switching circuitry or based on a multi-stage switching network constructed from a recursive 2-stage construction, said construction having a configuration based on one of the implementation levels, and

a second switching element, coupled to the first switching element, being a primitive switching circuitry or based on a multi-stage switching network constructed from a

recursive 2-stage construction, said construction having a configuration based on one of the implementation levels compatible with the first switching element.

12. (Previously presented) The switch as recited in claim 11 wherein the implementation levels include: inside-chip implementation, orthogonal packaging, interface board packaging, and fiber array packaging.

13. (Currently amended) A switch based upon a plurality of opto-electrical-physical implementation levels comprising:

n first switching elements implemented by a recursive 2-stage construction technique, each of the first switching elements having m output ports and having a configuration based on a first one of the implementation levels,

m second switching elements implemented by a recursive 2-stage construction technique, each of the second switching elements having n input ports and having a configuration based on a second one of the implementation levels, where m is not equal to n, and

an interface circuit interposed between the n first switching elements and the m second switching elements, wherein each of the first switching elements has a configuration based on a first one of the implementation levels compatible with the interface circuit and each of the second switching elements has a configuration based on a second one of the implementation levels also compatible with the interface circuit, the interface circuit having: mn input ports to cooperatively interconnect with the mn outputs

of the n first switching elements; nm output ports to cooperatively interconnect with the nm inputs of the m second switching elements; and interconnections between the mn input ports and the mn output ports corresponding to a pre-determined exchange.

14. (Previously presented) The switch as recited in claim 13 wherein the pre-determined exchange corresponds to an output exchange relative to the first switching elements.

15. (Previously presented) The switch as recited in claim 13 wherein the pre-determined exchange corresponds to an input exchange relative to the second switching elements.

16. (Previously presented) The switch as recited in claim 13 wherein the pre-determined exchange corresponds to an output exchange relative to the first switching elements as well as an input exchange relative to the second switching elements.

17. (Previously presented) The switch as recited in claim 13 wherein the first switching elements are stacked in n parallel first planes and wherein the second switching elements are stacked in m parallel second planes orthogonal to the first planes.

18. (Previously presented) The switch as recited in claim 13 wherein the implementation levels include: inside-chip implementation, printed circuit board implementation, orthogonal packaging, interface-board packaging, and fiber-array packaging.

19. (Currently amended) A switch comprising:
 n first $m \times m$ switching elements based on a first multi-stage network constructed from a recursive 2-stage construction technique, the first switching elements being stacked in n parallel first planes, each of the first switching elements having m outputs,
 m second $n \times n$ switching elements based on a second multi-stage network constructed from the recursive 2-stage construction technique with reference to the first switching elements, the second switching elements being stacked in m parallel second planes, each of the second switching elements having n outputs, and
 an interface circuit interposed between the n first switching elements and the m second switching elements, the interface circuit having: m input ports in each of n input planes parallel with the first planes to cooperatively interconnect with the m outputs of each of the first switching elements; n output ports in each of m output planes parallel with the second planes to cooperatively interconnect with the n inputs of each of the second switching elements; and interconnections between the mn input ports and the nm output ports corresponding to a pre-determined exchange.

20. (Previously presented) The switch as recited in claim 19 wherein the pre-determined exchange corresponds to an output exchange relative to the first switching elements.

21. (Previously presented) The switch as recited in claim 19 wherein the pre-determined exchange corresponds to an input exchange relative to the second switching elements.

22. (Previously presented) The switch as recited in claim 19 wherein the pre-determined exchange corresponds to an output exchange relative to the first switching elements as well as an input exchange relative to the second switching elements.

23. (Currently amended) A method for physically implementing a switch based upon a plurality of opto-electrical-physical implementation levels comprising:

implementing n first switching elements, each of the first switching elements having m output ports and a switching fabric which either is a primitive switching circuitry or has a configuration based on a first one of the implementation levels,

implementing m second switching elements, coupled to the n first switching elements, each of the second switching elements having n input ports where n is not equal to m , and a switching fabric which either is a primitive switching circuitry or has a configuration based on a second one of the implementation levels compatible with the first switching elements , and

configuring a 2-stage interconnection of the n first switching elements and m second switching elements by one of the implementation levels, wherein the implementation of the 2-stage interconnection are compatible with the first switching elements and the second switching elements.

24. (Previously presented) The method as recited in claim 23 wherein the 2-stage interconnection corresponds to an output exchange relative to the first switching elements.

25. (Previously presented) The method as recited in claim 23 wherein the 2-stage interconnection corresponds to an input exchange relative to the second switching elements.

26. (Previously presented) The method as recited in claim 23 wherein the 2-stage interconnection corresponds to an output exchange relative to the first switching elements as well as an input exchange relative to the second switching elements.

27. (Previously presented) The method as recited in claim 23 further including stacking the first switching elements in n parallel first planes and stacking the second switching elements in m parallel second planes orthogonal to the first planes.

28. (Previously presented) The method as recited in claim 23 wherein the implementation levels include: inside-chip implementation, printed circuit board implementation, orthogonal packaging, interface-board packaging, and fiber-array packaging.